WHAT IS CLAIMED IS:

1. A semiconductor device comprising memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a thickness of 30 nm or greater at the bottom portion thereof.

2. A semiconductor device comprising memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film and has a thickness of 30 nm or greater at the bottom portion thereof.

3. A semiconductor device comprising memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film and has a thickness of 30 nm or greater at the bottom portion thereof and a thickness of at least 30 nm or less at a side portion thereof.

4. A semiconductor device comprising memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a columnar shape having a cavity in a center portion thereof, and a minimum distance between said cavity and said first metal layer is 30 nm or greater.

5. The semiconductor device according to any one of claims 1 to 4, wherein said lower electrode has a thickness of 30 nm or greater at least at that portion which contacts said first metal layer.

6. The semiconductor device according to any one of claims 1 to 4, wherein at that portion of said lower electrode which contacts said first metal layer, there are at most three grain boundaries penetrating said lower electrode in a direction of thickness.

7. The semiconductor device according to any one of claims 1 to 4, wherein a crystal of said lower electrode at that portion of said lower electrode which contacts said first metal layer has at least 70% of a (002) orientation.

8. A semiconductor device comprising memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and a second metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film, said first metal layer and said second metal layer partly contact each other, said lower electrode is connected at an entire bottom thereof to said second metal layer

and said lower electrode has a thickness of 30 nm or greater at the bottom portion thereof.

9. A semiconductor device comprising memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and a second metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a shape of cups provided along side walls and bottoms of holes provided in an interlayer insulating film, said first metal layer and said second metal layer partly contact each other, said lower electrode is connected at an entire bottom thereof to said second metal layer and said lower electrode has a thickness of 30 nm or greater at the bottom portion thereof and a thickness of at least 30 nm or less at a side portion thereof.

10. A semiconductor device comprising memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and a second metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said first metal layer and said second metal layer partly contact each other, said lower electrode is connected at an entire bottom thereof to said second metal layer, said lower electrode has a columnar shape having a cavity in a center portion thereof and a minimum distance between said cavity and said second metal layer is 30 nm or greater.

11. The semiconductor device according to any one of claims 8 to 10, wherein said lower electrode has a thickness of 30 nm or greater at least at that portion which contacts said second metal lay r.

12. The semiconductor device according to any one of claims 8 to 10,

wherein at that portion of said lower electrode which contacts said second metal layer, there are at most three grain boundaries penetrating said lower electrode in a direction of thickness.

13. The semiconductor device according to any one of claims 8 to 10, wherein a crystal of said lower electrode at that portion of said lower electrode which contacts said second metal layer has at least 70% of a (002) orientation.

14. The semiconductor device according to any one of claims 8 to 10, wherein said second metal layer is a titanium nitride film.

15. The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said lower electrode is a metal film.

16. The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said lower electrode is a ruthenium film.

17. The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said lower electrode is a titanium nitride film.

18. The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said capacitive insulating film is a titanium nitride film.

19. The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said upper electrode is a ruthenium film.

20. The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said first metal layer is a titanium nitride film.

21. The semiconductor device according to any one of claims 1 through 4 and claims 8 through 10, wherein said first metal layer is a tungsten film.

22. A fabrication method for a semiconductor device comprising memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

said method comprising the steps of:

forming an interlayer insulating film on said first metal layer;

boring a hole in said interlayer insulating film to expose said first metal layer at a bottom portion of said hole;

forming said lower electrode whose thickness at that portion which contacts the first metal layer at that portion which contacts the first metal layer is greater than a thickness of the other portion;

forming said capacitive insulating film;

reforming said capacitive insulating film; and

forming said upper electrode.

23. A fabrication method for a semiconductor device comprising memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film, said method comprising the steps:

forming an interlayer insulating film on said first metal layer;

boring a hole in said interlayer insulating film to expose said first metal layer at a bottom portion of said hole;

forming said lower electrode whose thickness at that portion which contacts the first metal layer at that portion which contacts the first metal layer is greater than a thickness of the other portion;

forming said capacitive insulating film;

reforming said capacitive insulating film; and

forming said upper electrode.

24. A fabrication method for a semiconductor device comprising memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a

lower electrode having a columnar shape having a cavity in a center portion thereof and electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film, said method comprising the steps of:

forming an interlayer insulating film on said first metal layer;

boring a hole in said interlayer insulating film to expose said first metal layer at a bottom portion of said hole;

forming said lower electrode which satisfies a relationship of (a minimum distance between said cavity in said lower electrode and said first metal layer) ≥ 30 nm;

forming said capacitive insulating film;

reforming said capacitive insulating film; and

forming said upper electrode.

25. The fabrication method according to claim 24, wherein said step of forming said lower electrode has a step of burying said hole bored in said interlayer insulating film with a film for forming said lower electrode in such a way as to satisfy a relationship of (a minimum distance between a cavity in said second metal layer and said first metal layer) ≥ 30 nm.

26. The fabrication method according to any one of claims 22 to 24, wherein said step of boring a hole in said interlayer insulating film takes place once from said step of forming said interlayer insulating film to said step of forming said capacitive insulating film.

27. The fabrication method according to any one of claims 22 to 24, wherein in said step of forming said lower electrode, the thickness of said lower electrode at the bottom portion thereof is greater than the thickness of said lower electrode at a side portion thereof.

28. The fabrication method according to any one of claims 22 to 24, wherein in said step of forming said lower electrode, the thickness of said lower

electrode at the bottom portion thereof is 30 nm or greater and the thickness of said lower electrode at the side portion thereof does not exceed at least 30 nm.

29. The fabrication method according to any one of claims 22 to 24, wherein in said step of forming said lower electrode, the thickness of that portion of said lower electrode which contacts said first metal layer is greater than the thickness of the other portion.

30. The fabrication method according to any one of claims 22 to 24, wherein in said step of forming said lower electrode, the thickness of at least that portion of said lower electrode which contacts said first metal layer is 30 nm or greater and the thickness of said lower electrode at the side portion thereof does not exceed at least 30 nm.

31. A fabrication method for a semiconductor device which comprises memory cells each having an MISFET for memory selection formed on one major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and a second metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film in which said first metal layer and said second metal layer partly contact each other and said second metal layer partly contacts said lower electrode, said method comprising the steps of:

forming an interlayer insulating film on said first metal layer;

boring a hole in said interlayer insulating film to expose said first metal layer at a bottom portion of said hole;

forming said second metal layer in said bottom portion of said hole;

forming said lower electrode;

forming said capacitive insulating film;

reforming said capacitive insulating film; and

forming said upper electrode.

32. The fabrication method according to claim 31, wherein in said step

of forming said lower electrode, the thickness of at least that portion of said lower electrode which contacts said second metal layer is 30 nm or greater and the thickness of said lower electrode at the side portion thereof does not exceed at least 30 nm.

33. The fabrication method according to claim 31 or 32, wherein said second metal layer is a titanium nitride film.

34. The fabrication method according to any one of claims 22 to 24 and 31, wherein said first metal layer is a titanium nitride film.

35. The fabrication method according to any one of claims 22 to 24 and 31, wherein said first metal layer is a tungsten film.

36. The fabrication method according to any one of claims 22 to 24 and 31, wherein said lower electrode is a metal film.

37. The fabrication method according to any one of claims 22 to 24 and 31, wherein said lower electrode is a ruthenium film.

38. The fabrication method according to any one of claims 22 to 24 and 31, wherein said lower electrode is a titanium nitride film.

39. The fabrication method according to any one of claims 22 to 24 and 31, wherein said capacitive insulating film includes a tantalum oxide film.

40. The fabrication method according to any one of claims 22 to 24 and 31, wherein said upper electrode is a metal film.

41. The fabrication method according to any one of claims 22 to 24 and 31, wherein said upper electrode is a ruthenium film.

42. The fabrication method according to any one of claims 22 to 24 and 31, wherein said step of forming said lower electrode includes both a step of depositing a metal film by sputtering and a step of depositing a metal film by CVD.

43. The fabrication method according to any one of claims 22 to 24 and 31, wherein said step of forming said lower electrode includes a step of depositing a metal film by PCM sputtering.

44. The fabrication method according to any one of claims 22 to 24 and 31, wherein said step of forming said lower electrode includes a step of depositing a metal film by collimate sputtering.

45. The fabrication method according to any one of claims 22 to 24 and 31, wherein said step of reforming said capacitive insulating film is a heat treatment step.

46. The fabrication method according to any one of claims 22 to 24 and 31, wherein said step of reforming said capacitive insulating film is a heat treatment step which is performed in a hydrogen atmosphere.

47. The fabrication method according to any one of claims 22 to 24 and 31, wherein said step of reforming said capacitive insulating film is a heat treatment step which is performed in an ozone atmosphere.

48. The fabrication method according to any one of claims 22 to 24 and 31, wherein said step of reforming said capacitive insulating film is a heat treatment which is performed in an oxygen atmosphere at a temperature of 360°C or higher and 460°C or lower.